CLAIMS

What is claimed is:

1. A method of fabricating a metal-oxide semiconductor (MOS) transistor having an elevated source/drain structure, comprising:

forming a gate dielectric on an active region of a semiconductor substrate and forming a gate electrode on the gate dielectric;

forming a first gate spacer on lateral side surfaces of the gate electrode;

forming a first epi-layer on the semiconductor substrate;

forming a second gate spacer on lateral side surfaces of the first gate spacer; and

forming a second epi-layer on the first epi-layer.

2. The method as set forth in claim 1, further comprising:

forming a first gate oxide on the lateral side surfaces of the gate electrode before the first gate spacer is formed; and

forming a second gate oxide on the lateral side surfaces of the first gate spacer before the second gate spacer is formed.

3. The method as set forth in claim 1, further comprising:

forming a first poly-layer on the gate electrode while the first epi-layer is formed; and

forming a second poly-layer on the first poly-layer while the second epi-layer is formed.

4. The method as set forth in claim 1, further comprising:

ion-implanting a dopant in the semiconductor substrate to form a source/drain extension layer after the first epi-layer is formed; and

ion-implanting a dopant in the semiconductor substrate to form a deep source/drain layer after the second epi-layer is formed.

5. The method as set forth in claim 1, wherein a thickness of the first epi-layer is about 20 to 30 % of a combined thickness of an elevated source/drain layer formed by the first epi-

layer and the second epi-layer.

6. The method as set forth in claim 1, wherein a thickness of the second epi-layer is about 70 to 80 % of a combined thickness of an elevated source/drain layer formed by the first epi-layer and the second epi-layer.

7. The method as set forth in claim 1, wherein the second gate spacer is four to six times wider than the first gate spacer.

8. The method as set forth in claim 1, wherein at least one of the first epi-layer and second epi-layer comprises silicon.

9. The method as set forth in claim 8, wherein at least one of the first epi-layer and second epi-layer is grown in accordance with a low pressure chemical vapor deposition process.

10. The method as set forth in claim 9, wherein at least one of the first epi-layer and second epi-layer is formed using a source gas including dichlorosilane and HCl.

11. The method as set forth in claim 9, wherein the low pressure chemical vapor deposition process is conducted under 10 to 30 torr.

12. The method as set forth in claim 8, wherein at least one of the first epi-layer and second epi-layer is grown in accordance with an ultra-high vacuum chemical vapor deposition process.

13. The method as set forth in claim 12, wherein at least one of the first epi-layer and second epi-layer is formed using a source gas, including Si_2H_6.

14. The method as set forth in claim 12, wherein the ultra-high vacuum chemical vapor deposition process is conducted under 10^{-4} to 10^{-5} torr.

15. The method as set forth in claim 8, further comprising:

baking the semiconductor substrate or the first epi-layer at 800 to 900℃ under a hydrogen atmosphere for one to five minutes before the at least one of the first epi-layer and second epi-layer is formed.

16. The method as set forth in claim 1, wherein at least one of the first epi-layer and second epi-layer comprises silicon-germanium.

17. The method as set forth in claim 16, wherein at least one of the first epi-layer and second epi-layer is grown in accordance with a low pressure chemical vapor deposition process.

18. The method as set forth in claim 17, wherein at least one of the first epi-layer and second epi-layer is formed using a source gas, including dichlorosilane, HCl, and GeH_4.

19. The method as set forth in claim 17, wherein the low pressure chemical vapor deposition process is conducted under 10 to 30 torr.

20. The method as set forth in claim 16, wherein at least one of the first epi-layer and second epi-layer is grown in accordance with a ultra-high vacuum chemical vapor deposition process.

21. The method as set forth in claim 20, wherein at least one of the first epi-layer and second epi-layer is formed using a source gas, including dichlorosilane, HCl, and GeH_4.

22. The method as set forth in claim 20, wherein the ultra-high vacuum chemical vapor deposition process is conducted under 10^{-4} to 10^{-5} torr.

23. The method as set forth in claim 16, further comprising:

baking the semiconductor substrate or the first epi-layer at 800 to 900℃ under a

hydrogen atmosphere for one to five minutes before the first epi-layer or second epi-layer is formed.

24. The method as set forth in claim 1, further comprising forming a source/drain layer by in-situ doping a dopant in at least one of the first epi-layer and second epi-layer during forming the first epi-layer or second epi-layer.

25. The method as set forth in claim 1, further comprising forming a source/drain layer by ion-implanting a dopant in at least one of the first epi-layer or second epi-layer during forming the first epi-layer or second epi-layer.

26. A metal-oxide semiconductor (MOS) transistor having an elevated source/drain structure, comprising:

a gate dielectric formed on an active region of a semiconductor substrate;

a gate electrode formed on the gate dielectric;

a first gate spacer formed on a lateral side surfaces of the gate electrode;

a first epi-layer formed on the semiconductor substrate;

a second gate spacer formed on lateral side surfaces of the first gate spacer; and

a second epi-layer formed on the first epi-layer.

27. The MOS transistor as set forth in claim 26, further comprising:

a first gate oxide between the gate electrode and the first gate spacer; and

a second gate oxide between the first gate spacer and the second gate spacer.

28. The MOS transistor as set forth in claim 26, further comprising a poly-layer on the gate electrode.

29. The MOS transistor as set forth in claim 28, wherein a width of the poly-layer on the gate electrode is wider than a width of the gate electrode.

30. The MOS transistor as set forth in claim 28, wherein the poly-layer on the gate

electrode comprises silicon.

31. The MOS transistor as set forth in claim 28, wherein the poly-layer on the gate electrode comprises germanium.

32. The MOS transistor as set forth in claim 26, further comprising:

a source/drain extension layer formed by a dopant ion-implanting process, said source/drain extension layer being positioned under the first epi-layer and partially overlapped by a lower portion of the gate electrode; and

a deep source/drain layer formed by deeply ion-implanting a dopant in a portion of the semiconductor substrate positioned under the second epi-layer.

33. The MOS transistor as set forth in claim 26, wherein a thickness of the first epi-layer is about 20 to 30 % of a combined thickness of an elevated source/drain layer formed by the first epi-layer and the second epi-layer.

34. The MOS transistor as set forth in claim 26, wherein a thickness of the second epi-layer is about 70 to 80 % of a combined thickness of an elevated source/drain layer formed by the first epi-layer and the second epi-layer.

35. The MOS transistor as set forth in claim 26, wherein at least one of the first epi-layer and second epi-layer comprises silicon.

36. The MOS transistor as set forth in claim 26, wherein the second gate spacer is four to six times wider than the first gate spacer.

37. The MOS transistor as set forth in claim 26, wherein at least one of the first epi-layer and second epi-layer comprises silicon-germanium.